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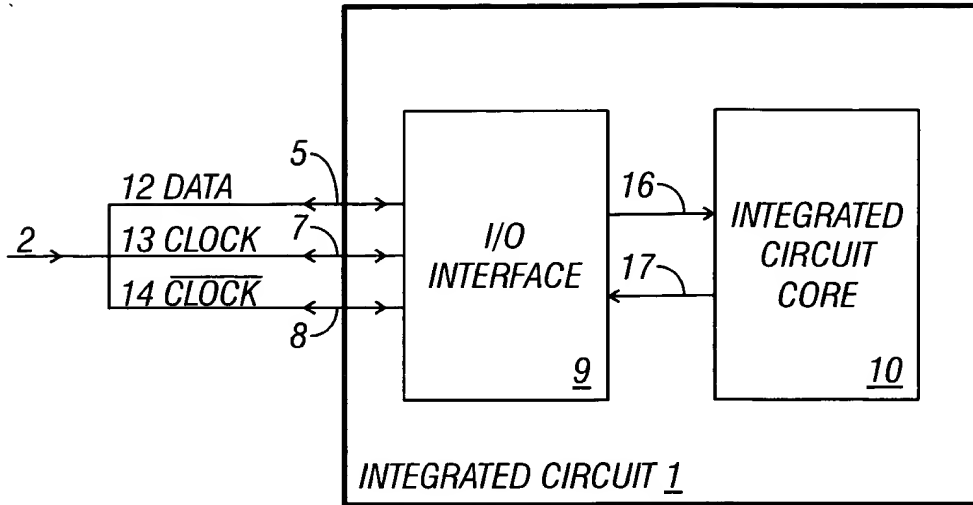


FIG. 1

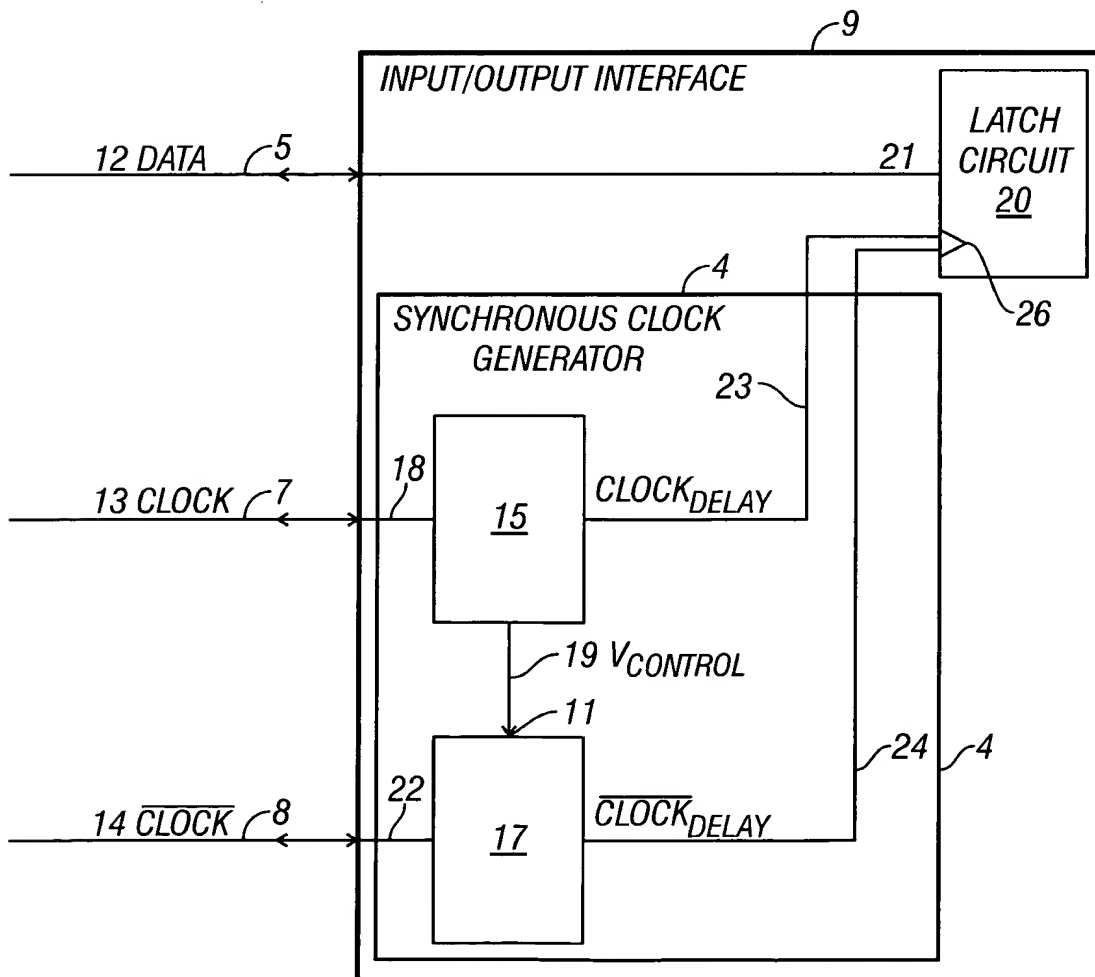


FIG. 2



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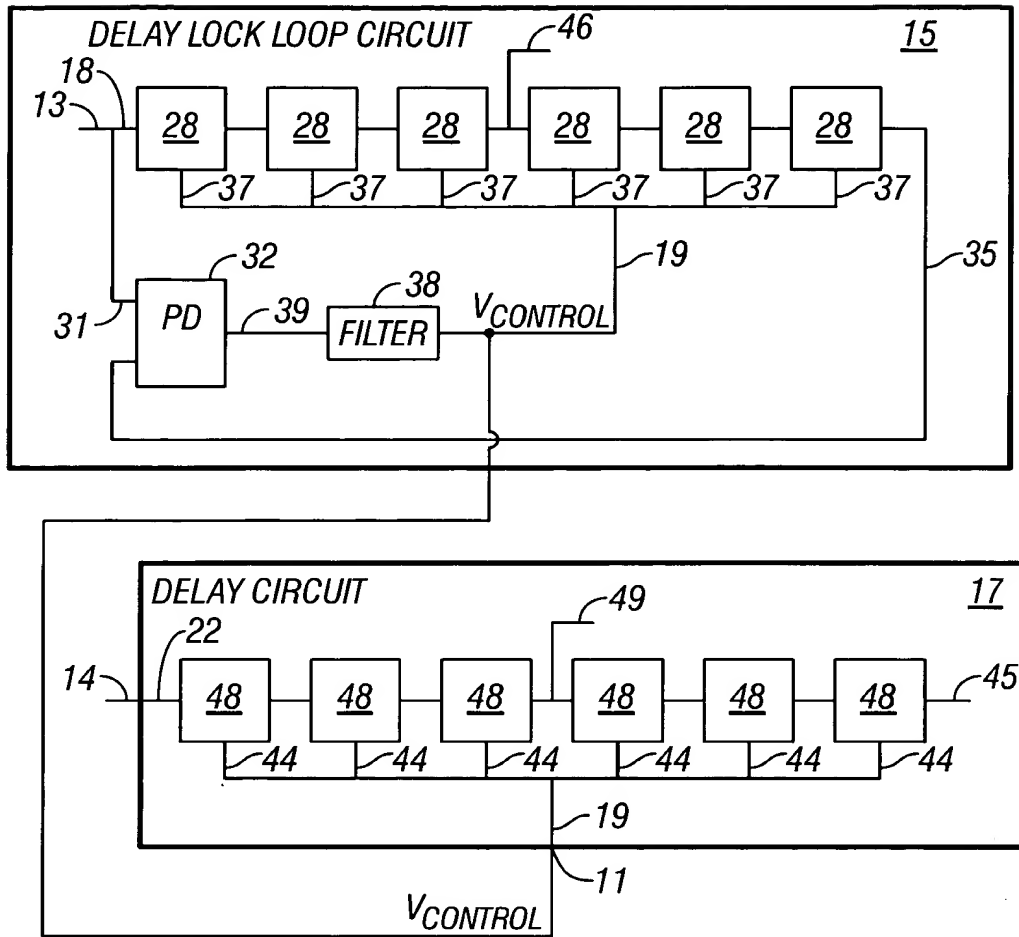


FIG. 3

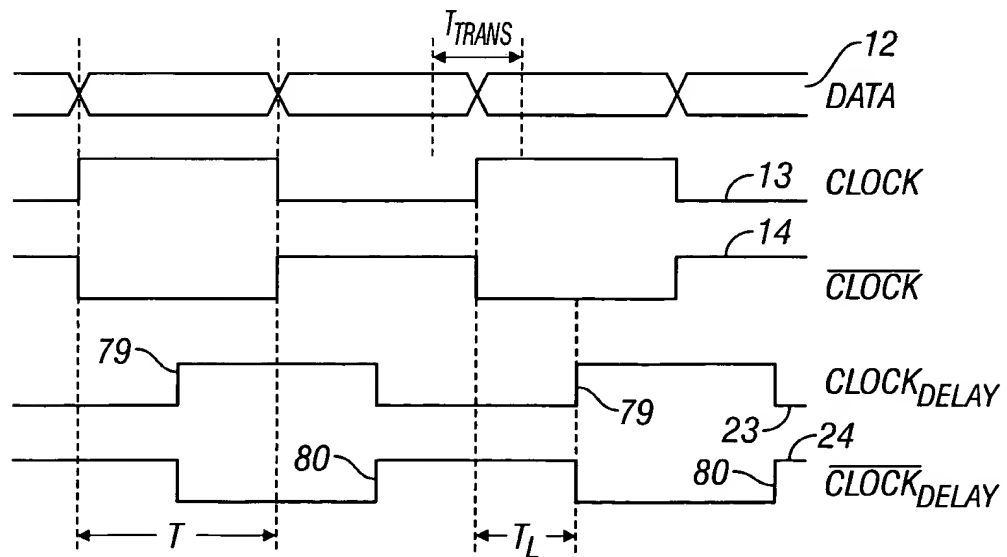


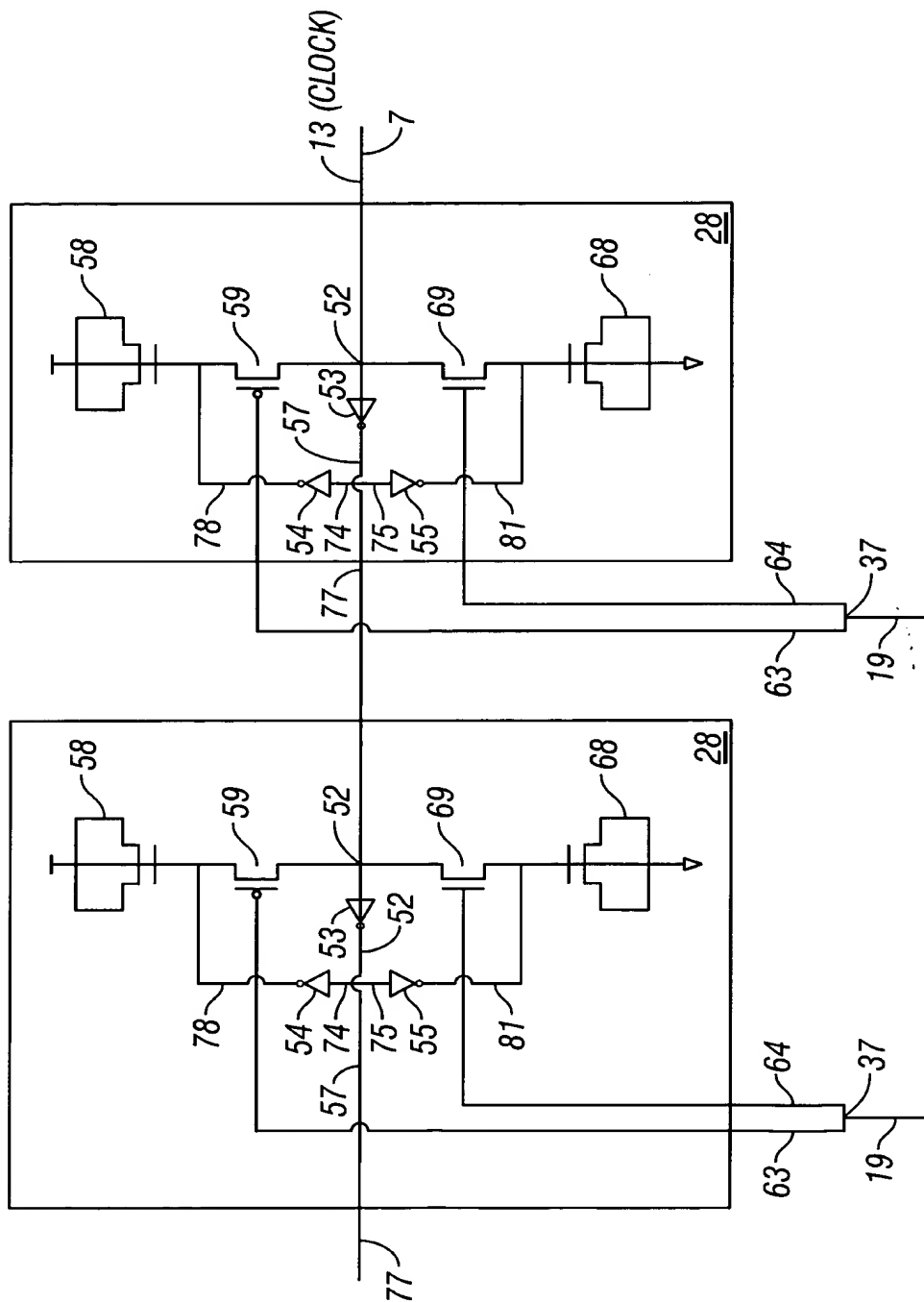
FIG. 5

Applicants: Shekhar Y. Borkar et al.

**A SYNCHRONOUS CLOCK GENERATOR FOR INTEGRATED CIRCUITS**

Replacement Sheet

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**FIG. 4**